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(54) **Self-programming scanning radio receiver.**

(57) Self-programming scanning receiver having superheterodyne circuitry, microprocessor controlled synthesized frequency tuning circuitry, frequency validation means, a learn mode to invoke the frequency validation means for all frequencies tunable by the tuning circuitry, listen mode for scanning of frequencies learned in the learn mode, and an ignore mode for erasing frequencies from permanent memory. The frequency validation means comprises a detector output connected to a high pass filter input, high pass filter output connected to a noise detector, noise detector output connected to a first A/D converter input, algorithms stored in microprocessor program memory for analyzing A/D samples obtained via first A/D for squelch condition, detector output also supplying the input of a low pass filter, output of low pass filter connected to a second A/D converter input, algorithms for analysis of A/D samples obtained from second A/D to determine sufficiency of modulation level and lack of digital waveforms, electrically alterable permanent memory for storing information identifying voice channels.

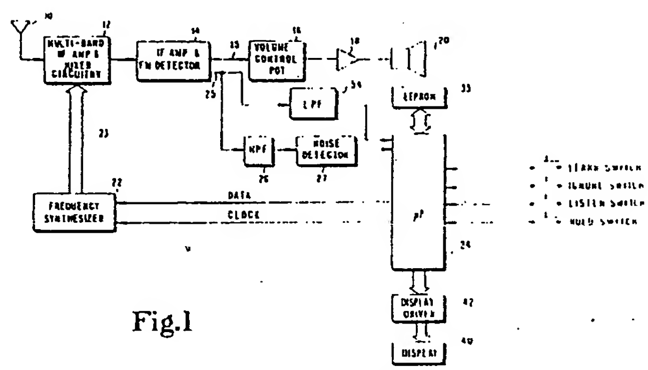

Fig.1

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SELF-PROGRAMMING SCANNING RADIO RECEIVER

Background of the Invention

This invention relates to scanning radio receivers, and more particularly to programmable scanning radio receivers.

Early scanning receivers used crystals for tuning, and the number of channels available for reception was limited to the number of crystals in a given receiver. A receiver typically contained either eight or sixteen crystals, and different crystals had to be installed to enable reception of different frequencies, including the frequencies of other desired transmissions within range of the receiver as well as, in the case of relocation or portable operation, the assigned frequencies in a different geographical region.

The versatility of scanning receivers was greatly enhanced with the advent of frequency synthesizers for generation of local oscillator frequencies. The frequency synthesizer is controlled by frequency codes stored in memory, and typically the memory can be reprogrammed for operation on different frequencies. It is also known to store a large number of frequency codes in memory, or alternatively to generate consecutive frequency codes as a function of known channel spacings. Increasing the number of tunable frequencies reduces the need for reprogramming, but it can also cause delays in tuning and increase the susceptibility to spurious signals commonly referred to as "birdies".

Delays in tuning occur because a finite time is required for a frequency synthesizer to lock onto each new frequency and for a squelch circuit to detect presence or absence of activity on the tuned frequency. If there are many tunable frequencies and the receiver stops on each one, the time delay between successive stops on a given channel of interest can become excessive even if no other channel is active.

Birdies are internally generated signals which conventional scanning receivers recognize as active frequencies. This false recognition causes conventional scanners to stop scanning and remain tuned to that frequency, even though no audio modulation is present. When a scanner tunes to a momentarily inactive or locally unused frequency, a time delay is introduced, as mentioned above, but scanning resumes afterward. In the case of birdies, however, the scanner locks up and external intervention is required to release the scanner for further scanning.

Summary of the Invention

The present invention overcomes these and other disadvantages of the prior art by providing a self-programming scanning radio receiver including means operative during a first mode of operation for automatically tuning the receiver to a plurality of radio frequencies, means for producing a receiver signal in response to each radio frequency to which the receiver is tuned, voice detection means for analyzing each receiver signal and identifying therefrom the radio frequencies carrying voice information, and scan means operative during a second mode of operation for automatically sequentially tuning the receiver to the radio frequencies identified by the voice detection means as carrying voice information.

It is a general object of the present invention to provide an improved programmable scanning radio receiver.

It is a further object of the present invention to provide a self-programming scanning receiver capable of ascertaining which radio frequencies carry voice information and storing for later scanning recall each validated frequency.

These and other objects and advantages of the present invention will become more apparent upon reading the following detailed description of the preferred embodiment in conjunction with the accompanying drawings.

Brief Description of the Drawings

FIG. 1 is a block diagram of the preferred embodiment of the scanning radio receiver according to the present invention.

FIG. 2 is a flowchart of the "birdie" recognition program used in the receiver of FIG. 1 to detect the presence or absence of modulation on the currently tuned radio frequency.

FIG. 3 is a flowchart of the subroutine called in the program of FIG. 2.

FIG. 4 is a flowchart of the program which determines whether digital data is present in the signal received by the scanning radio receiver of FIG. 1.

Description of the Preferred Embodiment

For the purposes of promoting an understand-

ing of the principles of the invention, reference will now be made to the embodiment illustrated in the drawings and specific language will be used to describe the same. It will nevertheless be understood that no limitation of the scope of the invention is thereby intended, such alterations and further modifications in the illustrated device, and such further applications of the principles of the invention as illustrated therein being contemplated as would normally occur to one skilled in the art to which the invention relates.

With reference to FIG. 1, the preferred embodiment of a scanning radio receiver according to the present invention includes an antenna 10 coupled to a conventional superheterodyne FM receiver which includes RF amplifier and mixer circuitry 12, an IF amplifier and FM detector 14, a volume control potentiometer (pot) 16, mode control switches, an audio amplifier 18 and a speaker 20. The RF amplifier and mixer circuitry 12 includes individual RF amplifiers and mixers for the low and high VHF bands as well as the UHF band, as well as appropriate tracking circuits. The local oscillator signal for the receiver is generated by frequency synthesizer 22, which also supplies tracking signals to the three RF amplifiers and performs band switching as required. Multi-band RF amplifier and mixer circuitry such as that just described is well known in the art and does not require detailed description.

High-pass filter 26 is the first stage of a squelch circuit which also includes a noise detector 27 whose output is connected to the input of an A/D converter of microprocessor 24. Microprocessor 24 analyzes the signal from noise detector 27 to determine whether a carrier has been received by antenna 10. If only high frequency audio signals are detected by the squelch circuit, carrier is presumed absent, and the microprocessor 24 will mute the audio and resume frequency scanning. A number of forms of squelch circuits would be appropriate for use in conjunction with the present invention, and several suitable forms are disclosed in U.S. Patent Application Serial No. 21,008 filed March 2, 1987, which application is hereby incorporated by reference.

The scanning receiver depicted in FIG. 1 has the following functional operating modes: LEARN mode, LISTEN mode, HOLD mode, and IGNORE mode. Each mode is activated by the closure of a switch connected to the microprocessor as shown in FIG. 1. In LEARN mode the receiver programs an internal memory with, or learns, the frequency information used during scanning, i.e., LISTEN mode.

When microprocessor 24 detects closure of the LEARN switch, it enters the LEARN mode in which synthesizer 22 is sequentially tuned to all frequencies which the receiver is capable of receiving. For each tuned frequency, microprocessor 24 evaluates the demodulated audio signal, if it is sufficient to open squelch, and determines from characteristics of that signal whether or not the current channel is a voice channel. More specifically, frequencies modulated to a predetermined extent and determined not to be carrying digital data are considered voice channels by the microprocessor and are identified accordingly in memory for later scanning recall. A predetermined bit in EEPROM 33 is set for each analyzed radio frequency determined to be carrying voice information, and only those frequencies are scanned during LISTEN mode. Another set of bits is provided in memory for designating which frequencies have already been analyzed.

Microprocessor 24 monitors the output signal from IF amplifier and FM detector 14 after that signal is filtered through first-order lowpass filter (LPF) 54, which has a corner frequency of approximately 12 kHz. High-speed A/D sampling of the filter output signal is executed by microprocessor 24, using an internal A/D converter, at a rate of 13.8 kHz. As will be described, microprocessor 24 is programmed to execute a birdie check routine in which it acquires a predetermined number of samples of the filter output and determines therefrom the extent of modulation. The microprocessor determines the sum of the absolute values of the deviations of the respective samples from the average sample value, and then compares that cumulative absolute value with a predetermined threshold. A data detection program is also executed if the analyzed frequency passes the birdie check, i.e., if it is determined not to be a birdie.

FIG. 2 depicts the program stored in internal read-only memory (ROM) of the microprocessor, executed upon actuating the LEARN switch of FIG. 1 activating microprocessor 24 of FIG. 1 to enter the LEARN mode and scan the entire frequency range of the receiver, testing each signal tuned for validity as to minimal modulation. A variable stored in RAM of microprocessor 24 representing the program loop iteration counter of the birdie loop is zeroed in step 100. The birdie subroutine is called in step 102. Upon return from the birdie subroutine, the program tests the data returned from the birdie subroutine instep 104. If a birdie is detected by the birdie subroutine (see FIG. 3), program step 108 executes causing a delay of a predetermined amount of time before the program tests the number of calls which have occurred. If the birdie routine has been called five times, the loop is completed and the program continues to step 112. If the birdie routine has not been called five times, the program returns to step 102, and the loop executes again. Once the birdie subroutine step

102 has been called five times, and five results have been obtained as determined in step 110, the program proceeds to step 112 and tests for more than three birdie confirmations received from the birdie subroutine of FIG. 3. If four or more responses from the birdie subroutine are affirmative, then the program executes step 114 indicating a birdie has been tuned by the receiver tuning circuitry FIG. 1, and a bit is set in memory 33 by microprocessor 24 corresponding to the radio frequency tuned by the receiver. Should the birdie count be three or less the program continues with step 116, rather than 114, and no bit is set. Program flow returns to the calling program after step 114 or 116.

Referring to FIG. 3, the flowchart for the birdie subroutine functions as follows. The detected audio signal produced by the FM detector, after passing through lowpass filter 54, is monitored through an A/D input of microprocessor 24, FIG. 1. At step 150 a memory pointer, labeled slot pointer, is cleared and thereby set to the lowest address provided in a random-access memory (RAM) internal to microprocessor 24 for the A/D samples. At Step 152 the voltage from lowpass filter 54 is converted into a digital number which, in step 154, is summed with the current sum of all digital numbers obtained in step 152 for the current execution of the routine. At step 156 the current digital number is stored in the memory location currently designated by the slot pointer. The slot pointer is incremented at step 158 and the loop counter for steps 152 through 160 is tested for 32 executions of the loop. If steps 152 through 160 have not yet executed 32 times, the program returns to step 152 and continues. If 32 executions of step 152 to 160 loop have occurred, step 162 executes after step 160, dividing the sum calculated in step 154 by 32, thereby averaging the A/D readings obtained in steps 150 through 160.

At step 164 the sum variable and the slot pointer are cleared. At step 166 the microprocessor reads the first location of memory set aside for A/D samples, and then, in step 168, it determines whether or not the current reading is greater than the average reading determined in step 162. If greater than the average, step 172 executes and sum is set equal to the information stored in sum plus the memory slot reading minus the average reading. If the A/D reading pointed to by slot or memory pointer is less than or equal to the average from step 162, then, at step 170, sum is set equal to sum plus the average minus the slot value. The slot pointer is incremented at step 174, and at step 176 the program determines whether or not 32 executions of the program loop (steps 166 through 176) have occurred. If less than 32, the program returns to step 166 and the loop from step 166 through 174 is executed again by the microprocessor. If 32 or more loops from step 166 through step 174 have been completed then the conditional branch instruction in step 176 forces program execution to continue to step 178.

At step 178, microprocessor 24 tests the value stored in the memory location designated sum and determines if it is greater than 256. If so, the program continues to step 182 and sets a modulation indicator flag in RAM indicating the presence of modulation. If the result in step 178 conditional block is no, then the modulation flag in RAM is reset in step 180 indicating that the output of the FM detector has an insufficient AC component for genuine modulation. After the modulation flag is set or reset in steps 182 or 180, respectively, the program returns to step 104 of FIG. 2.

FIG. 4 illustrates the subroutine flowchart for the program activated by a call to the square wave detector subroutine. At step 200 microprocessor 24 takes 32 consecutive A/D readings of the filtered FM detector output signal and stores those readings in RAM. At Step 201 the samples obtained in step 200 are normalized so that the lowest reading in the 32 samples is set to zero as the reference and the other 31 samples are adjusted downward in value by the value of the smallest reading. At step 202 the program tests whether or not a square wave signal was sampled in step 200. The signal is considered to be a square wave if 24 or more of the 32 normalized samples from step 201 are either less than 1/4, or greater than 3/4, of the value of the largest reading of the 32. If the samples satisfy this test, the program continues at step 203 and a memory flag is set indicating that digital data has been detected in the 32 samples taken in this call to subroutine. Otherwise, data is considered not present for this call.

Steps 200 through 203 are repeated, or called, 64 times, in four groups, or sections, of 16 calls. The number of calls is monitored in step 204. The results of each call and each section are stored and then analyzed in step 205 to determine whether digital data is present on the currently tuned channel. For a channel to be considered as carrying digital data, digital data must be found present in at least one of the 16 calls in three of the four sections. That is, for each section, there must be a data-present indication for at least one of the 16 calls. The use of four sections prevents falsing, and the use of 16 calls to obtain one true indication allows for noise. If these required conditions are met in step 205, program control returns to the calling routine with a memory flag set indicating that the currently tuned radio frequency is modulated with digital data. If not, program control returns with the flag not set.

LEARN mode causes microprocessor 24 to initiate a program to analyze all tunable frequencies

of the receiver for squelch open condition, modulation in the detected signal, and digital data. Unless squelch is open while the receiver is tuned to a particular frequency, the birdie and square wave routines will not execute with respect to that frequency. Also, if the birdie check reveals a birdie, the square wave routine will not execute; the channel is determined not to be a voice channel, and the receiver initiates tuning to the next frequency to be checked. After the receiver has tuned to all frequencies once, the receiver automatically switches to LISTEN mode and begins scanning.

LEARN mode can be subsequently activated for a second pass by again depressing the LEARN switch. This feature is useful for detecting voice channels which, due to momentary inactivity or some other reason, were previously untested. In subsequent passes, only channels which were previously identified as voice are not retested. If it is desired to delete a channel from the scan list, such is accomplished on an individual basis using the IGNORE switch. All channels can be deleted by depressing the IGNORE switch and holding it down while power is switched on to the receiver.

The HOLD switch is used to stop scanning and thereby hold the receiver tuned to the current frequency for an indefinite period. The receiver stays in HOLD mode until the HOLD switch is again closed or until the receiver is turned off.

While the invention has been illustrated and described in detail in the drawings and foregoing description, the same is to be considered as illustrative and not restrictive in character, it being understood that only the preferred embodiment has been shown and described and that all changes and modifications that come within the spirit of the invention are desired to be protected.

Claims

1. A self-programming scanning radio receiver, comprising:
heterodyne receiver means for frequency conversion and detection of a signal modulated on an RF carrier;
frequency synthesizer means for supplying a local tuning oscillator signal to said heterodyne receiver, said frequency synthesizer means having a frequency code input;
frequency code generation means for supplying frequency codes to said frequency code input;
memory means for storing a plurality of frequency codes, said memory means having an output coupled to said frequency code input;
frequency validation means for analyzing a detected signal on a frequency corresponding to one of said frequency codes supplied to said frequency code input, said frequency validation means including means for automatically recognizing signals representing voice information;
means for automatically loading said memory means with frequency codes corresponding to frequencies determined to be valid by said frequency validation means.

2. The self-programming scanning radio receiver of claim 1 wherein said frequency validation means includes an A/D converter means for obtaining multiple A/D samples of the detected signal.

3. The self-programming scanning radio receiver of claim 2 wherein said frequency validation means includes a low pass filter means for filtering high frequencies from said detected signal and connecting the output of said low pass filter to said A/D converter means input.

4. The self-programming scanning radio receiver of claim 3 wherein said frequency validation means includes digital analysis means for computing an average for said A/D samples and summing the absolute value of the difference between each sample and the average sample value resulting in an absolute value difference sum which is compared to a predetermined value.

5. The self-programming scanning radio receiver of claim 4 wherein said digital analysis means obtains multiple sets of said A/D samples and multiple absolute value difference sums are computed for each set of said A/D samples by said digital analysis means and further analysis by said digital analysis means occurs such that a majority of said absolute value difference sums must exceed a predetermined value.

6. The self-programming scanning radio receiver of claim 5 wherein said frequency validation means obtains from said A/D convertor multiple A/D convertor samples of said low pass filter output and said digital analysis means reduces all samples by the least value sample and compares said samples to a lower and upper range limit said range limits determined as a function of the reduced sample with the highest value, with a determination that digital data is present in the detected signal based upon a predetermined percentage of reduced samples found to be greater than said upper range limit or less than said lower range limit.

7. The self-programming scanning radio receiver of claim 6 wherein said digital analysis means obtains multiple sets of samples from said A/D converter and for each sample set said digital analysis reduces all samples by the smallest sample value of the sample set and compares each sample of the set to said lower and said upper range limits computed for each set said digital

analysis summing the number of sets meeting the range check and comparing the sum to a predetermined value.

8. The self-programming scanning radio receiver of claim 7 wherein said frequency validation means stores validation results by setting a bit corresponding to the frequency in said memory means indicating an invalid frequency thereby informing said frequency code generation means not to tune to said invalid frequency while said scanning radio receiver is scanning for active radio frequencies.

9. The self-programming scanning radio receiver of any one of the preceding claims, wherein said frequency code generation means (33) includes second memory means for storing a plurality of codes corresponding to tunable frequencies, said codes defining a set of frequencies which are automatically checked by said frequency validation means (24).

10. The self-programming scanning radio receiver of any one of the preceding claims, wherein means for a second or subsequent frequency validation occurs and said frequency validation means (24) operates only on those frequencies not previously identified as voice frequency and stored in said memory means (33).

11. The self-programming scanning radio receiver of any one of the preceding claims, further comprising means for resetting all bits in said memory means (33) corresponding to all frequencies determined invalid by said frequency validation means.

12. The self-programming scanning radio receiver of claim 3, wherein said low pass filter (54) is a first-order filter with a corner frequency of approximately 13.8 kilohertz.

13. The self-programming scanning radio receiver of claim 2, wherein aid A/D converter means (24) can perform a conversion in approximately 72 microseconds, and said A/D converter means can provide 32 samples in approximately 2.3 milliseconds.

14. A self-programming scanning radio receiver, comprising:

a) means (24,22) operative during a first mode of operation for automatically tuning said receiver to a plurality of radio frequencies;

b) means (12,14) for producing a receiver signal in response to each radio frequency to which said receiver is tuned;

c) voice detection means (24,54) for analyzing each receiver signal and identifying therefrom the radio frequencies carrying voice information; and

d) scan means (24) operative during a second mode of operation for automatically sequentially tuning said receiver to the radio frequencies identified by said voice detection means as carrying voice information.

15. The self-programming scanning radio receiver of claim 14, wherein said voice detection means includes means (54,24) for recognizing birdies.

16. The self-programming scanning radio receiver of claim 14 or 15, wherein said voice detection means includes means (54,24) for recognizing digital data signals.

17. The self-programming scanning radio receiver of any one of claims 14 to 16, further comprising squelch means (26,27) for inhibiting said voice detection means (24) in the absence of a detected signal.

18. The self-programming scanning radio receiver of any one of claims 14 to 17, wherein said voice detection means (24) checks a frequency only once per invocation of said first mode of operation.

19. The self-programming scanning radio receiver of any one of claims 14 to 18, wherein said voice detection means includes means (24) for recognizing digital data signals.

20. A method of automatically programming a scanning radio receiver, comprising the steps:

a) automatically tuning said receiver to a plurality of radio frequencies during a first mode of operation;

b) generating a receiver signal in response to a radio frequency to which said receiver is tuned;

c) automatically distinguishing between voice information and other characteristics of said receiver signal; and

d) storing identifying information in a scanning memory for radio frequencies on which voice information is detected in said distinguishing step.

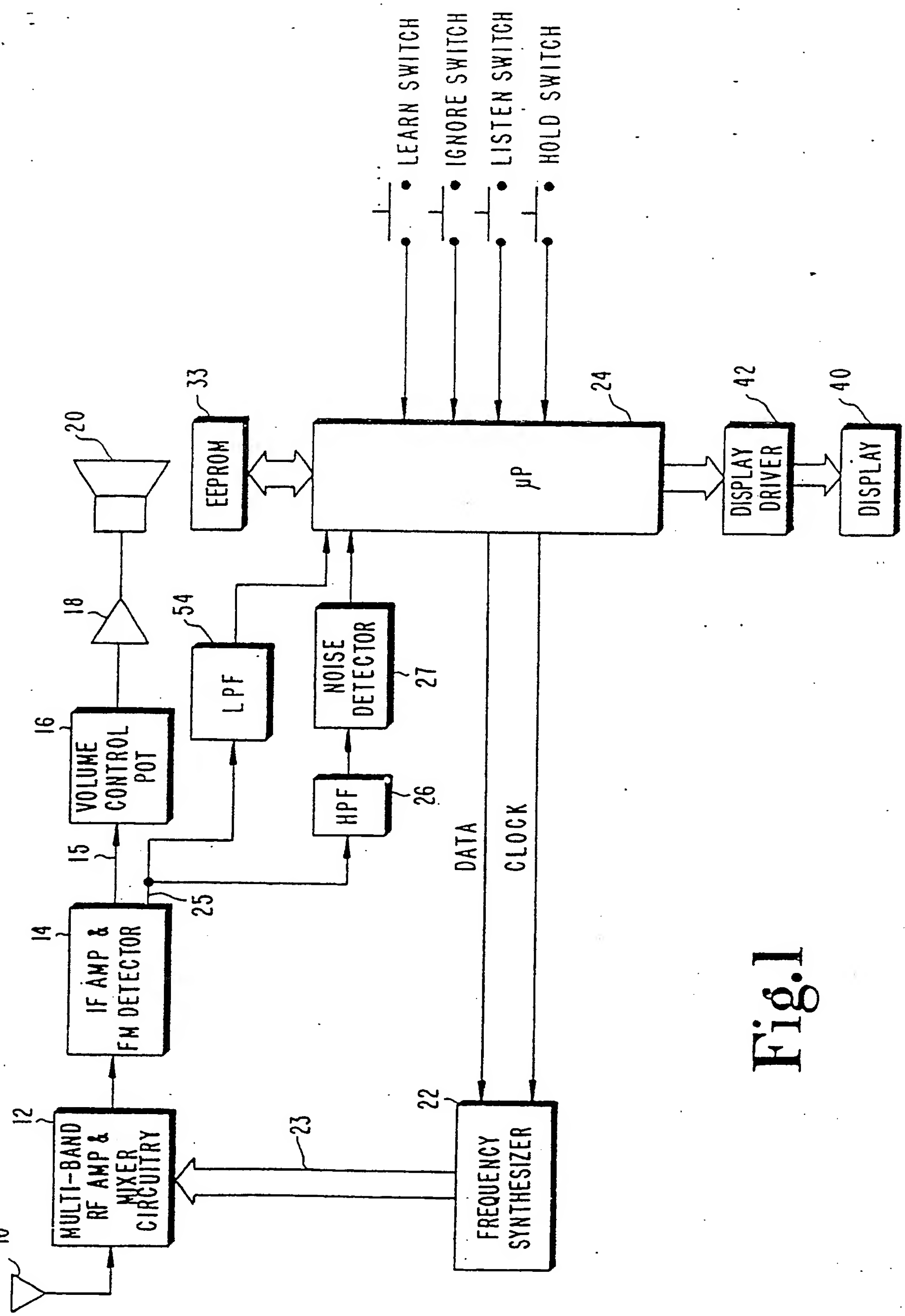
LEARN SWITCH
IGNORE SWITCH
LISTEN SWITCH
HOLD SWITCH
20
33
EEPROM
24
μP
42
DISPLAY DRIVER
40
DISPLAY
18
54
LPF
NOISE DETECTOR
27
16
VOLUME CONTROL POT
HPF
26
15
DATA
CLOCK
14
IF AMP &
FM DETECTOR
25
12
MULTI-BAND RF AMP & MIXER CIRCUITRY
23
22
FREQUENCY SYNTHESIZER
10

Fig.1

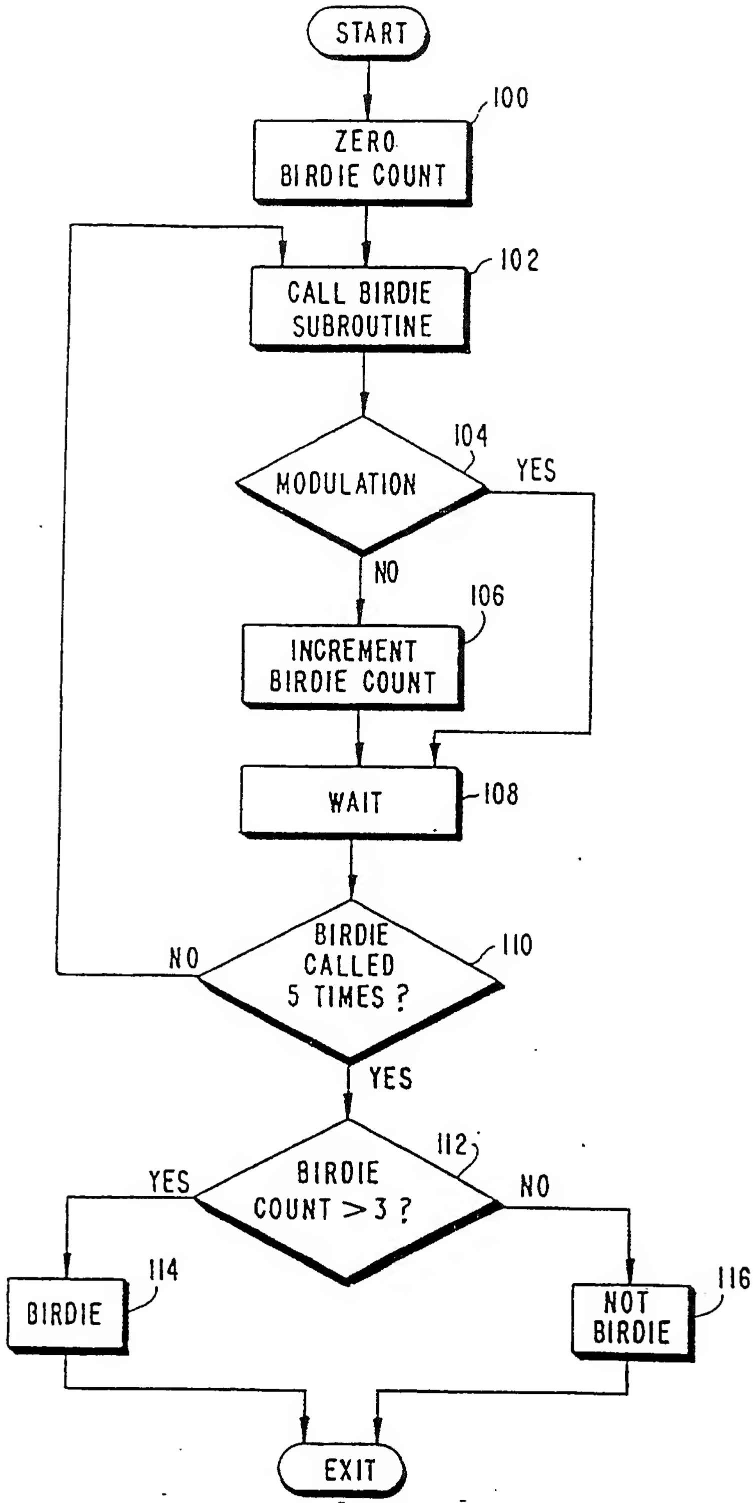
START
100
ZERO
BIRDIE COUNT
102
CALL BIRDIE
SUBROUTINE
104
MODULATION
YES
NO
106
INCREMENT
BIRDIE COUNT
WAIT
108
NO
BIRDIE
CALLED
5 TIMES ?
110
YES
112
YES
BIRDIE
COUNT > 3 ?
NO
114
BIRDIE
116
NOT
BIRDIE
EXIT

Fig.2

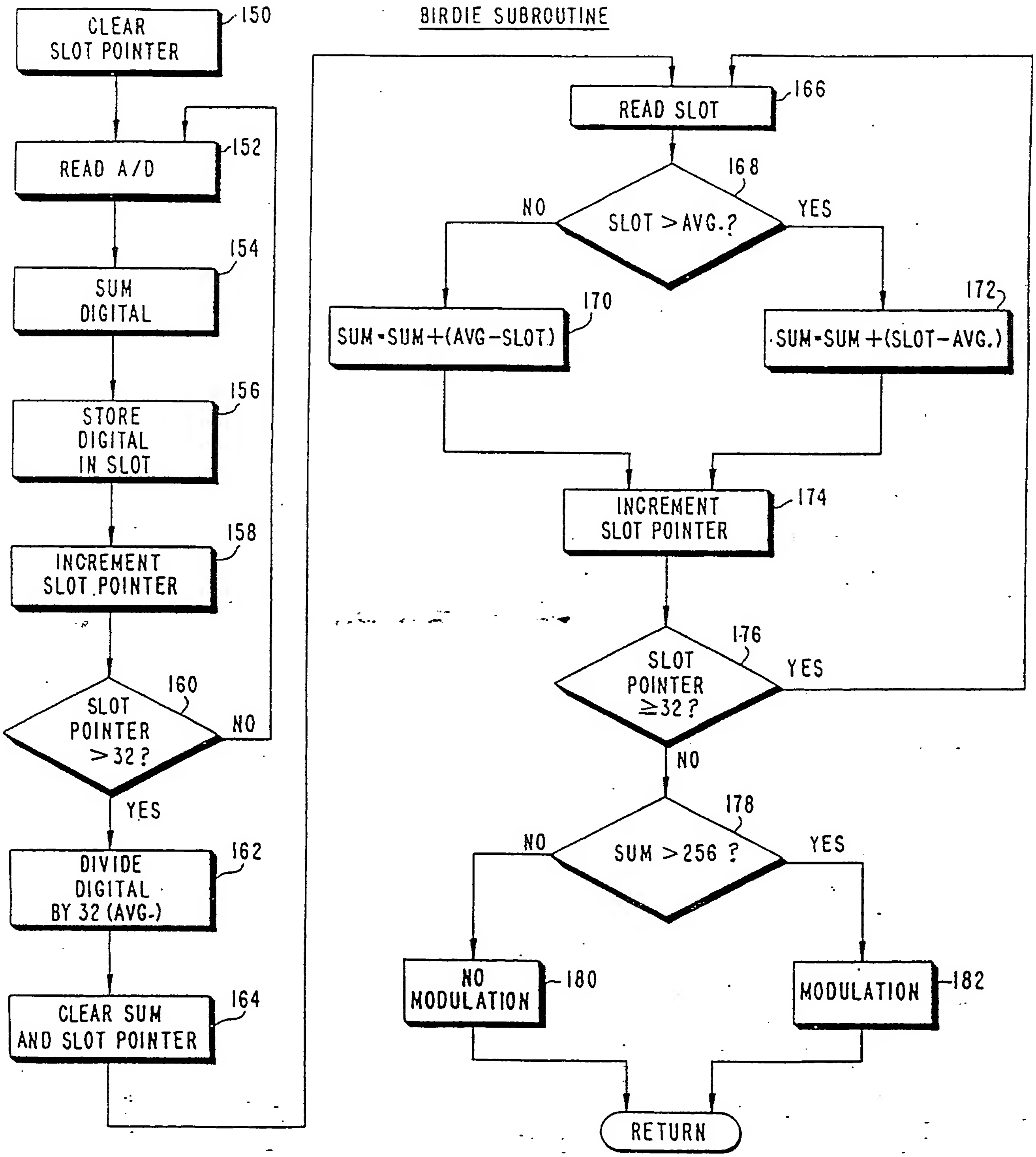
CLEAR SLOT POINTER
150
READ A/D
152
SUM DIGITAL
154
STORE DIGITAL IN SLOT
156
INCREMENT SLOT POINTER
158
SLOT POINTER >32?
160
NO
YES
DIVIDE DIGITAL BY 32 (AVG.)
162
CLEAR SUM AND SLOT POINTER
164
BIRDIE SUBROUTINE
READ SLOT
166
SLOT > AVG.?
168
NO
YES
SUM=SUM+(AVG-SLOT)
170
SUM=SUM+(SLOT-AVG.)
172
INCREMENT SLOT POINTER
174
SLOT POINTER ≥32?
176
YES
NO
SUM >256 ?
178
NO
YES
NO MODULATION
180
MODULATION
182
RETURN

Fig.3

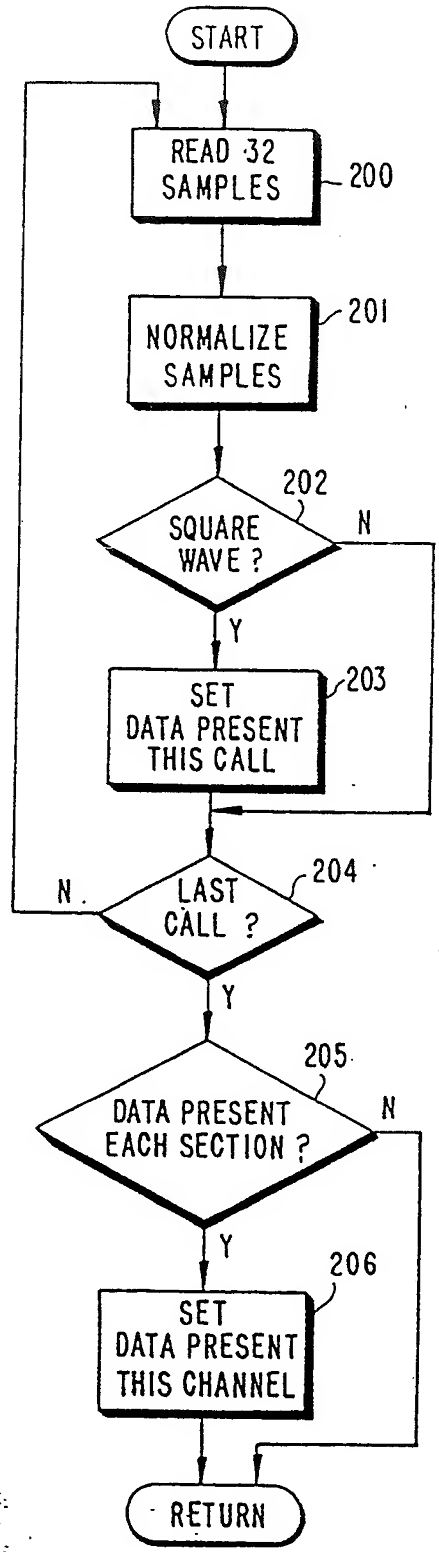
START
READ 32 SAMPLES
200
NORMALIZE SAMPLES
201
SQUARE WAVE ?
202
N
Y
SET DATA PRESENT THIS CALL
203
LAST CALL ?
204
N
Y
DATA PRESENT EACH SECTION ?
205
N
Y
SET DATA PRESENT THIS CHANNEL
206
RETURN

Fig.4